CLAIMS

Having thus described my invention, what I claim as new and desire to secure by Letters Patent is as follows:

1. A method of forming an asymmetric field effect transistor to control floating body effect, said method including steps of

defining a gate location with a trench in a dielectric layer on a semiconductor layer,

supplying impurities to said semiconductor layer at edges of said trench and adjacent source and drain regions, and

forming a gate structure on said semiconductor layer in said trench.

2. A method as recited in claim 1, including further steps of

removing said dielectric layer, and

forming source and drain impurity regions adjacent said gate structure.

3. A method as recited in claim 2, wherein said step of forming source and drain impurity regions is performed by impurity implantation.

4. A method as recited in claim 2, including a further step of

depositing an insulator layer over said source and drain regions and said gate structure.

5. A method as recited in claim 4, including a further step of

planarizing said insulator layer to said gate structure.

6. A method as recited in claim 1, wherein said gate location is defined between source and drain impurity regions.

7. A method as recited in claim 6, including a further step of

planarizing said gate structure to said dielectric layer.

8. A method as recited in claim 1, wherein said step of supplying impurities is performed by angled implantation within said trench.

9. A method as recited in claim 1, including the further step of forming a sidewall within said trench.

10. A method as recited in claim 1, wherein said sidewall is a doped material and said step of supplying impurities is performed by diffusion from said sidewall.

11. A method as recited in claim 1, wherein said semiconductor layer is formed on an insulator layer.

12. An asymmetric field effect transistor formed by a process including steps of

defining a gate location with a trench in a dielectric layer on a semiconductor layer,

supplying impurities to said semiconductor layer at edges of said trench and adjacent source and drain regions, and

forming a gate structure on said semiconductor layer in said trench.

13. A transistor as recited in claim 12, said process including further steps of

removing said dielectric layer, and

forming source and drain impurity regions adjacent said gate structure.

14. A transistor as recited in claim 13, wherein said step of forming source and drain impurity regions is performed by impurity implantation.

15. A transistor as recited in claim 13, said process including a further step of

depositing an insulator layer over said source and drain regions and said gate structure.

16. A transistor as recited in claim 15, said process including a further step of

planarizing said insulator layer to said gate structure.

17. A transistor as recited in claim 12, wherein said gate location is defined between source and drain impurity regions.

18. A transistor as recited in claim 17, said process including a further step of

planarizing said gate structure to said dielectric layer.

19. A transistor as recited in claim 12, wherein said step of supplying impurities is performed by angled implantation within said trench.

20. A transistor as recited in claim 12, said process including the further step of forming a sidewall within said trench.

21. A transistor as recited in claim 12, wherein said sidewall is a doped material and said step of supplying impurities is performed by diffusion from said sidewall.

22. A transistor as recited in claim 12, wherein said semiconductor layer is formed on an insulator layer.